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miss and (queue or buffer) and address and

[Advanced Scholar Search](#)[Scholar Preferences](#)[Scholar Help](#)Lowercase "or" was ignored. Try "OR" to search for either of two terms. [\[details\]](#)The "AND" operator is unnecessary -- we include all search terms by default. [\[details\]](#)Scholar All articles - [Recent articles](#)Results 1 - 10 of about 10,500 for [miss](#) and [\(queue or buffer\)](#) and [address and cache](#). (0.32 seconds)[Store queue for a tightly coupled multiple processor configuration with two-level cache buffer ...](#)SL Gregor - US Patent 5,023,776, 1991 - [freepatentsonline.com](#)

... if the search resulted in an L2 cache directory miss. ... write buffers and L2 store queues are all ... The aforementioned L2 write buffer controls (L2WB CTLs) are ...

[Cited by 90](#) - [Related articles](#) - [Web Search](#) - [All 6 versions](#)[Cache miss buffer adapted to satisfy read requests to portions of a cache fill in progress without ...](#)PN Patel, A Melony, Hix Hayes - US Patent 5,383,426, 1994 - [freepatentsonline.com](#)

... cause read signals and the physical address to be ... indicator in the instruction/data cache miss buffer, block 96 ... to be provided to the instruction queue, one of ...

[Cited by 31](#) - [Related articles](#) - [Web Search](#) - [All 3 versions](#)[Virtual address table look aside buffer miss recovery method and apparatus](#)RP Colwell, J O'Donnell, DB Papworth, PK Rodman - US Patent 4,920,477, 1990 - [freepatentsonline.com](#)

... illustrating the elements of the status queue data word in ... provides an indication of the cache miss read state ... PC data through a bidirectional buffer 299b over ...

[Cited by 13](#) - [Related articles](#) - [Web Search](#) - [All 2 versions](#)[History-based prefetch cache including a time queue](#)AD Beronbaum, TE Jorjanyan - US Patent 5,778,438, 1996 - [freepatentsonline.com](#)

... correlating an address of a cache miss with an event in the time queue and inserting the cache miss address into the prefetch target buffer indexed and ...

[Cited by 18](#) - [Related articles](#) - [Web Search](#) - [All 3 versions](#)[\[PDF\] ▶ The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 MHz](#)RE Kessler, MA Shrovesbury - IEEE, editor, Hot chips - [courses.ece.uiuc.edu](#)

... Int Issue Queue (20) Exec 4 Instructions / cycle ... 128-bit 44-bit Victim Buffer L1 Data Cache ... Addr Miss Address Branch Predictors Next-Line Address L1 Ins. Cache ...

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... caching, refetch cache lines starting at a cache miss address. The prefetched data is placed in the buffer and not in the cache. ...

[Cited by 1061](#) - [Related articles](#) - [Web Search](#) - [BI Direct](#) - [All 42 versions](#)[Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreading ...](#) - [▶ uiuc.edu](#) [PDF]HM Levy, JL Lo, JS Emer, Rl Stamm, SJ Eggers, DM ... - [ieeexplore.ieee.org](#)

... provided by a decoupled branch target buffer (BTB) and ... thousand instructions 3 5 9 L3 cache miss rate 55.1 ... cycles) 14% 9% 3% avg (combined) queue population 25 ...

[Cited by 617](#) - [Related articles](#) - [Web Search](#) - [BI Direct](#) - [All 57 versions](#)[UltraSPARC-III: designing third-generation 64-bit performance](#)T Horel, G Lauterbach, SM Inc, P Alto - Micro, IEEE, 1999 - [ieeexplore.ieee.org](#)

... path buffering in the I stage (the miss queue) ... of instructions; enqueue instructions into the queue J Steer ... and instruction address translation buffer access ...

[Cited by 95](#) - [Related articles](#) - [Web Search](#) - [BI Direct](#) - [All 7 versions](#)[Power and performance tradeoffs using various caching strategies](#) - [▶ virginia.edu](#) [PDF]RI Bahar, G Albera, S Manne - Low Power Electronics and Design, 1996 Proceedings, 1996 ... 1996 - [ieeexplore.ieee.org](#)

... associated with each first level cache; this buffer was implemented as ... Load/Store Queue Entries 16 Fetch Queue 16 Minimum ... 011 a miss, we use a write-back, write ...

[Cited by 103](#) - [Related articles](#) - [Web Search](#) - [All 8 versions](#)[Methods and apparatus for improving cache consistency using a single copy of a cache tag memory in ...](#)JH Chang, C Berg, J Cruz-Rios - US Patent 5,980,321, 1996 - [freepatentsonline.com](#)

... write, write-invalidate, and write-miss operations associated ... block to be written to the invalidation queue. ... also written to the output buffer holding pending ...

[Cited by 47](#) - [Related articles](#) - [Web Search](#) - [All 3 versions](#)Key authors: [N Jouspi](#) - [H Levy](#) - [R Kessler](#) - [J Lo](#) - [J Emer](#)

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